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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,151	12/01/2003	Min-Su Jeong	GK-US035197	1615
22919	7590	02/09/2007	EXAMINER	
GLOBAL IP COUNSELORS, LLP 1233 20TH STREET, NW, SUITE 700 WASHINGTON, DC 20036-2680			FILE, ERIN M	
		ART UNIT	PAPER NUMBER	
		2611		
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	02/09/2007	PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/724,151	JEONG ET AL.
Examiner	Art Unit	
Erin M. File	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 01 December 2003.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-19 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-19 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 01 December 2003 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 12/1/2003.

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .  
5)  Notice of Informal Patent Application  
6)  Other: \_\_\_\_ .

## DETAILED ACTION

### *Drawings*

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Independent Claim 1 states "a controller for calculating a variation in gain characteristics of the voltage controlled oscillator using the control voltage outputted from the voltage detector and the division rate of the divider". However, the drawings do not support the controller receiving the value of the division rate of the divider, and to the contrary, the specification states "Preferably, the division rate of the divider is set by the controller" (p. 5, lines 3-4), "The division rate N of the feedback divider 207 is decided on the basis of a fourth control signal Vc4 outputted from the controller 211" (p. 17, lines 21-24). Therefore, the contradictory features must be corrected or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Ballantyne (U.S. Patent No. 6,909,331).

**Claim 1**, Ballantyne discloses:

- a phase comparator for comparing phases of first and second signals applied thereto with each other and outputting a phase error signal when there is a phase difference between the two signals (col. 5, line 14-15, fig. 3, 304);
- a loop filter for filtering the phase error signal outputted from the phase comparator and stabilizing the filtered signal, to output a control signal (fig. 3, 108);
- a voltage controlled oscillator for controlling frequency gain of a signal outputted in response to the control signal outputted from the loop filter (fig. 3, 102);
- a divider for dividing the frequency of the output signal of the voltage controlled oscillator according to a division rate to apply it to the phase comparator as the second signal (fig. 3, 104);
- a voltage detector for detecting control voltage from the control signal of the voltage controlled oscillator (col. 1, lines 65-67); and
- a controller for calculating a variation in gain characteristics of the voltage controlled oscillator using the control voltage outputted from the voltage detector and the division rate of the divider, and adjusting gain of the voltage controlled oscillator, to control gain of a loop composed of the phase comparator, the loop filter, the voltage controlled oscillator and the divider to be substantially uniform (fig. 3, 106, col. 1, line 65-col. 2, line 13, voltage controller 106 detects a voltage

in response to voltage divider 104 which adjusts the output voltage to correct VCO 102, see fig. 3 for loop, phase comparator 304, loop filter 108, and VCO 102).

**Claim 4**, Ballantyne discloses the loop filter includes a variable gain amplifier, and voltage gain of the loop filter is controlled by adjusting a gain value of the variable gain amplifier (col. 4, lines 34-36).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantyne (U.S. Patent No. 6,909,331) as applied to claim 1 above, and further in view of Oka (U.S. Pub. No. 2001/0036239).

**Claim 2**, Ballantyne fails to disclose the division rate of the divider is set by the controller, however, Oka discloses the division rate of the divider is set by the controller ([0037], lines 4-7). Oka further discloses that the variation of frequency division rate allows for smoothing of the variation in the frequency of the clock signal ([0015], lines 3-7). Because of this advantage, it would have been obvious to one skilled in the art at the time of invention to incorporate the frequency division rate control as disclosed by

Oka into the invention of Ballantyne.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantyne (U.S. Patent No. 6,909,331) as applied to claim 1 above, and further in view of Ichimaru (U.S. Patent No. 6,593,783).

**Claim 5**, Ballantyne fails to disclose the voltage detector is composed of an analog-digital converter, however, Ichimaru discloses a capacitor for voltage detection including an analog to digital converter (col. 7, lines 58-63). The use of analog to digital converters are well known in the art because of the ease and efficiency with which digital signals can be manipulated. Because of this advantage, it would have been obvious to one skilled in the art at the time of invention to incorporate the analog to digital conversion as disclosed by Ichimaru into the invention of Ballantyne.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantyne (U.S. Patent No. 6,909,331) as applied to claim 1 above, and further in view of Chappell (U.S. Patent No. 6,425,132).

**Claim 6**, Ballantyne fails to disclose the voltage controlled oscillator includes at least two voltage controlled oscillators, and one of the voltage controlled oscillators is activated according to a control signal provided by the controller. Chappell discloses a voltage controlled oscillator includes at least two voltage controlled oscillators, and one of the voltage controlled oscillators is activated according to a control signal provided by

the controller (fig. 4, 242, 246, col. 7, lines 8-20). MOTIVATION

9. Claims 8, 10, 12, 14, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groen et al. (U.S. Patent No. 6,683,502) in view of Nakamura (U.S. Patent No. 6,792,064).

**Claim 8**, Groen discloses:

- a first step of setting the division rate of the divider to a predetermined first division rate (fig. 8, 810), and;
- a second step of setting the division rate of the divider to a predetermined second division rate, and detecting control voltage from the control signal (fig. 8, 860); and
- a third step of calculating the frequency gain of the voltage controlled oscillator (col. 4, lines 16-18, discloses  $K_{VCO}$  is the frequency gain) using the frequency of the first signal, the control voltages, the first and second division rates.

Groen fails to disclose control voltages detected at first and second steps, however, Nakamura discloses control voltage detecting unit after the frequency division operation (col. 8, lines 1-6). Because Nakamura discloses that his implantation of a phase locked loop mechanism has the advantage of increasing the reliability of its operations (col. 6, lines 1-10), it would have been obvious to one skilled in the art at the time of invention to incorporate the voltage control detector as disclosed by Nakamura into the invention of Groen.

**Claim 10**, Groen discloses:

- a first step of setting the frequency of the output signal of the voltage controlled oscillator to a predetermined first frequency (fig. 8, step 810, Groen discloses setting the VCO to 0);
- a third step of controlling the division rate of the divider to vary the frequency of the output signal of the voltage controlled oscillator by a predetermined frequency value (fig. 8, 860, col. 5, lines 43-45),
- a fourth step of calculating the frequency gain of the voltage controlled oscillator using the predetermined frequency value (fig. 8, 850, col. 5, lines 64-66); and
- a fifth step of comparing the frequency of the output signal of the voltage controlled oscillator with a predetermined second frequency and repeatedly performing the second and fourth steps until the frequency of the output signal has a value identical to the second frequency value (fig. 8, 870, 880, col. 6, lines 9-21).

Groen fails to disclose control voltages detected at first, second, and third steps, however, Nakamura discloses control voltage detecting unit after the frequency division operation (col. 8, lines 1-6). Because Nakamura discloses that his implantation of a phase locked loop mechanism has the advantage of increasing the reliability of its operations (col. 6, lines 1-10), it would have been obvious to one skilled in the art at the time of invention to incorporate the voltage control detector as disclosed by Nakamura into the invention of Groen.

**Claim 12**, Groen discloses:

- a first step of detecting a control voltage value from the control signal at a predetermined reference frequency;
- a second step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by a predetermined specific frequency and detecting control voltage from the control signal;
- a third step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by the specific frequency and detecting control voltage from the control signal; and
- a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages respectively detected at the second and third steps and the frequency of the output signal.

Groen fails to disclose control voltages detected at first, second, and third steps, however, Nakamura discloses control voltage detecting unit after the frequency division operation (col. 8, lines 1-6). Because Nakamura discloses that his implantation of a phase locked loop mechanism has the advantage of increasing the reliability of its operations (col. 6, lines 1-10), it would have been obvious to one skilled in the art at the time of invention to incorporate the voltage control detector as disclosed by Nakamura into the invention of Groen.

**Claim 14**, Groen discloses:

- a first step of setting the frequency of the output signal of the voltage controlled oscillator to a predetermined first frequency (fig. 8, step 810, Groen discloses setting the VCO to 0);

- a third step of controlling the division rate of the divider to vary the frequency of the output signal of the voltage controlled oscillator by a predetermined frequency value (fig. 8, 860, col. 5, lines 43-45)
- a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages detected at the second and third steps and the predetermined frequency value (fig. 8, 850, col. 5, lines 64-66);
- a fifth step of comparing the frequency of the output signal of the voltage controlled oscillator with a predetermined second frequency and repeatedly performing the second and fourth steps until the frequency of the output signal has a value identical to the second frequency value (fig. 8, 870, col. 6, lines 9-11); and
- a sixth step of setting a desired output signal frequency of the voltage controlled oscillator and controlling gains of the phase comparator and loop filter (fig. 8, 880, col. 6, lines 11-21).

Groen fails to disclose control voltages detected at first, second, and third steps, however, Nakamura discloses control voltage detecting unit after the frequency division operation (col. 8, lines 1-6). Because Nakamura discloses that his implantation of a phase locked loop mechanism has the advantage of increasing the reliability of its operations (col. 6, lines 1-10), it would have been obvious to one skilled in the art at the time of invention to incorporate the voltage control detector as disclosed by Nakamura into the invention of Groen.

**Claim 16**, Groen discloses:

- a second step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by a predetermined specific frequency (fig. 8, 860, col. 5, lines 43-45);
- a third step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by the specific frequency and detecting control voltage from the control signal (fig. 8, 860, col. 5, lines 43-45)
- a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages respectively detected at the second and third steps and the frequency of the output signal (fig. 8, 850, col. 5, lines 64-66); and
- a fifth step of controlling gain of the phase comparator or gain of the loop filter, to control the loop gain to be substantially uniform (fig. 8, 880, col. 6, lines 11-21).

Groen fails to disclose control voltages detected at first, second, and third steps, however, Nakamura discloses control voltage detecting unit after the frequency division operation (col. 8, lines 1-6). Because Nakamura discloses that his implantation of a phase locked loop mechanism has the advantage of increasing the reliability of its operations (col. 6, lines 1-10), it would have been obvious to one skilled in the art at the time of invention to incorporate the voltage control detector as disclosed by Nakamura into the invention of Groen.

**Claim 18**, Groen discloses:

- a second step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by a predetermined specific frequency (fig. 8, 860, col. 5, lines 43-45);

- a third step of varying the frequency of the output signal of the voltage controlled oscillator from the reference frequency by the specific frequency and detecting control voltage from the control signal (fig. 8, 860, col. 5, lines 43-45)
- a fourth step of calculating the frequency gain of the voltage controlled oscillator using the control voltages respectively detected at the second and third steps and the frequency of the output signal (fig. 8, 850, col. 5, lines 64-66); and
- a fifth step of comparing the calculated frequency gain with a predetermined reference gain and controlling the frequency gain of the voltage controlled oscillator to be substantially uniform (fig. 8, 880, col. 6, lines 11-21).

Groen fails to disclose control voltages detected at first, second, and third steps, however, Nakamura discloses control voltage detecting unit after the frequency division operation (col. 8, lines 1-6). Because Nakamura discloses that his implantation of a phase locked loop mechanism has the advantage of increasing the reliability of its operations (col. 6, lines 1-10), it would have been obvious to one skilled in the art at the time of invention to incorporate the voltage control detector as disclosed by Nakamura into the invention of Groen.

#### ***Claim Rejections - 35 USC § 112***

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Examples of this include:

In Claim 7, the recitation "includes at least one inductor and capacitor that determine a frequency band, and frequency gain of the voltage controlled oscillator is varied by controlling an impedance value of the inductor or capacitor" lacks structural agreement. It is suggested that what is meant is "includes at least one of *an* inductor and capacitor that determine a frequency band, and frequency gain of the voltage controlled oscillator is varied by controlling an impedance value of the inductor or *the* capacitor"

In Claim 8 "using the frequency of the first signal, the control voltages, the first and second division rates". It is unclear whether this is meant to include all the limitations, or is it intended to be a Markush type of Claim.

In Claim 14, "grasping the frequency gain of the voltage controlled oscillator at the corresponding frequency as a value calculated through the first to fifth steps" the term grasping as used here is unclear.

13. In Claim 6, the recitations "the voltage controlled oscillator includes at least two voltage controlled oscillators, and one of the voltage controlled oscillators is activated according to a control signal provided by the controller" is unclear. The voltage controlled oscillator including at least two voltage controlled oscillators creates an imprecise reference to "one of the voltage controlled oscillators".

14. Claim 8 recites the limitation "the first and second division rates" in line 24. Claim 10 recites the limitation "a predetermined frequency value" in line 22 and the limitation "the second frequency value" in line 32. Claim 12 recites the limitation "by the specific frequency" in line 23. Claim 16 recites the limitation "the specific frequency" in line 23.

There is insufficient antecedent basis for these limitations in the claims.

15. Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: in line 37 of Claim 14, the recitation "and controlling gains of the phase comparator and loop filter" is incomplete as it does not described how or in what manner the gains of the phase comparator and loop filter are controlled.

16. The term "substantially uniform" in claims 1, 16, and 18 is a relative term which renders the claim indefinite. The term "substantially uniform" is not defined by the

claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

17. In claims 16 and 18, the recitations of the second step and the third step are almost identical except that in the second step a predetermined specific frequency is disclosed (in Claim 16, line 19), and in the third step the specific frequency (in Claim 16, line 23), both of which seems to be referring the same of frequency. It is unclear why this step is performed twice.

***Allowable Subject Matter***

18. Claims 3, 7, 9 11, 13, 15, 17, 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 1:00PM-9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571)272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Erin M. File

EMF

1/27/2007

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